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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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IBM CORPORATION
PO BOX 12195
DEPT 9CCA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,228	CORREALE ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to because, in figure 6, the control inputs of the transistors of (602) are not labeled; figures 1, 2 and 4 should be labeled "prior art"; the recitation "a restore mechanism" in claims 16 and 21; "a state saving latch" in claims 17 and 23 are not shown in the drawings.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1- 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitations "a first latch **adapted to** be coupled to a first power supply" and "a second latch coupled to the first latch and **adapted to** be coupled to a second power supply" are indefinite because it is unclear as to how the first and second latches are "**adapted** to be coupled to the first and second power supplies" According to the drawings the first and second latches are **coupled directly** to the first and second power supplies (V1, V2). The same analysis is true for the recitation "adapted to" in claims 11, 20, 23,

Regarding claim 2, the recitation "in a power saving mode, the voltage of at least one of the first and second power supplies **is reduced**" is indefinite because it is unclear how the voltage of the first or the second power supply can be reduced. Figures 6-8 show that the power supplies (V1) and (V2) are directly connected to the latches. There are **no devices or circuits** that are utilized to vary the power supply voltages as recited.

Regarding claim 3, the recitation "in a power saving mode, the voltage of the power supply coupled to the latch which contains contents to be preserved is **reduced** to a voltage to preserve the state of the contents and the other power supply is **reduced** to substantially zero volts" is indefinite for the same reason raised in the rejection of claim 2.

Regarding claims 17 and 23, the recitation " **a state saving latch**" is indefinite because it is misdescriptive. Figures 6-8 of the present application show only two latches: the master latch (602) and the slave latch (604). The Applicant is requested to show the "a state saving latch" in the drawings. It is also unclear as to the "state saving latch" on line 18 is the same or different than the "slave latch" on line 16.

Regarding claim 22, the recitation "a state saving latch" is indefinite because it not clear as to this "a state saving latch" is the same or different than the "slave latch in claim 20.

Regarding claim 24, the recitation "providing a first independently **controllable power supply** coupled to the first latch; (b) providing a second independently controllable power supply coupled to the second latch; and c) **reducing** the voltage of at least one of the first and second power supplies responsive to the detection of a power saving mode" is indefinite because it is misdescriptive. Figures 6-8 of the present application shows that there are no devices used to vary the supply voltages (V1) and (V2). The same analysis is true for the recitation "controllable power supply" in claim 29.

Regarding claim 29, the recitation "detecting the normal mode" is indefinite because it is unclear how a normal mode can be detected. There is no detection circuit shown in the drawings.

Claims 4-16, 18, 19, 21, 23 and 25-28 are indefinite because of the technical deficiencies of claims 1, 11, 20, and 24.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 18, 19 and 24-29, insofar as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi (US Pat. 6,433,586).

Regarding claims 1 and 2, figures 4, 6A, 6B and 7 show a flip-flop comprising:

a first latch (22) "adapted" to be coupled to a first power supply (PSO); and

a second latch (24) coupled to the first latch and adapted to be coupled to a second power supply (PS1), wherein the first and second power supplies are independently controllable to minimize power consumption when the flip-flop is in a power saving mode. Note that in the sleep mode (saving mode) the voltage of the first power supply (PS0) becomes 0 volt and the voltage of the second power supply (PS1) is coupled to the voltage (VBST), Node (NS1) is coupled to (VCC/2) for reducing the leakage current thus, the power consumption is minimized (col. 11, lines 37-49, col.14 lines 14-19).

Regarding claim 3, figures 6A, 6B, and 7 show that during the sleep mode, the supply voltage (PSO) of the master latch reduces to 0 volt and the control voltage (NS1) of the slave latch that preserves the data is raised to an intermediate voltage (VCC/2) thus, the power consumption of the master-slave flip-flop is reduced (col. 11, lines 37-50, col. 14, lines13-20).

Regarding claims 4, 5, 6 and 7, the first latch (22) is a master latch and the second latch (24) is a slave latch. The first clock is (TG1) and the second clock is (TG2). (TG1) and (TG2) are free running clocks.

Regarding claims 18 and 19, in the sleep mode, (PSO) is reduced to 0 volt and the voltage across the slave latch (24) that preserves the "contents" is reduced by bringing up the voltage at (NS1) to (VCC/2) (col.11, lines 43-49, col.14, lines 13-20).

Regarding claims 24 and 25, figures 4, 6A, 6B and 7 show a method for minimizing the power consumption of a flip-flop, the flip-flop including a first latch (22) and a second latch (24) coupled thereto; the method comprising the steps of:

(a) providing a first independently controllable power supply (PSO) coupled to the first latch;

(b) providing a second independently controllable power supply coupled to the second latch (PS1); and

c) reducing the voltage of at least one of the first (PS1 is reduced to volt) and second power supplies (PS1) responsive to the detection of a power saving mode. Note that in the power saving mode (sleep mode), (PS1) is reduced to 0 volt (col. 11, lines 37-49) and the voltage across the slave latch (24) is reduced by bringing up the voltage at (NS1) to VCC/2 (col. 14, lines 13-20). Thus, the power consumption of the flip-flop is reduced. Note that the slave latch (24) supplied by (PS1) that "preserves" the "contents" has the supply (PS1) is reduced by raising the voltage of (NS1) and supply (PS0) is reduced to 0 volt.

Regarding claims 26, 27 and 28, the first latch (22) is a master latch and the second latch (24) is a slave latch. The first clock is (TG1) and the second clock is (TG2).

Regarding claim 29, figures 4, 6A, 6B and 7 show a method for returning normal mode from power saving mode to preserve the contents in a flip-flop, the flip-flop including a first latch and a second latch coupled thereto, the method comprising the steps of:

(a) providing a first independently controllable power supply (PSO) coupled to the master latch (22);

b) providing a second independently controlling power supply (PS1) coupled to the second latch (24) wherein the at least one of the first and second power supplies is at substantially zero volts and the other of the first and second power supplies is at a reduced voltage such that the state of the contents in the associated latch is preserved;

(c) When the normal mode is desired the first and second power supplies is restore to full values (VCC) (col. 10, lines 47-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (US Pat. 6,433,586).

Regarding claims 8-10, figure 4 of Ooishi includes all the limitation of claims 8-10 except for the limitations that the first clock is gated and the second clock is free running; the first clock is free running and the second clock is gated. The first clock is gated and the second clock is gated. However, it is old and well known in the art that a gated clock coupled to a device is used to control that device by turning it on or by turned it off. By turning off the clock, the device is disabled. Therefore, it would have been obvious to those skilled in the art to implement the gate to the clocks of the flip-flops of Ooishi to control the functional modes of the flip-flop. For instance if the two gated clock are disabled, the flip-flop will stop working. The master-slave flip-flop works as a single latch if only one of the gated clock is enabled.

Claims 11, 12-17 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (US Pat. 6,433,586) in view of Barbier et al. (US Pat. 5,777,489).

Regarding claims 11, 12, 20 and 23, figures 4, 6A, 6B and 7 of Ooishi include all the limitations of the present application except for the limitation that there is a multiplexor coupled to the first and second latch. Figure 2 of Barbier shows a master-slave flip-flop having a multiplexor (208) coupled to the outputs of the master latch (204) and to the output of the slave latch (206) for selecting the output of the master latch or the slave latch for performing a desired function (col. 3, lines 48-67). Therefore, it would have been obvious to those skilled in the art to implement the multiplexor taught by Barbier to the master-slave circuit of Ooishi for the selection of the latch outputs. (208) is a shunt multiplexor. Note that in the sleep mode, the power supply (PSO) is reduced to 0 volt and the power supply (PS1) is reduced to a lower value by bringing the voltage at node (NS1) to (VCC/2) (See Ooishi col. 11and 14).

Regarding claims 13, 14, 15 and 16, figure 5 of Ooishi shows that during a first clock (TG1) one bit of data (D2) is latched by the first latch (22). The first latch (22) is a master latch and the second latch (24) is a slave latch. The "a restore mechanism" is the multiplexor (208).

Regarding claim 17, the "state saving latch" is element (24) that is activated only in the standby power mode (sleep mode). Note that in the sleep mode latch (22) is turned off and latch (24) is turned on with a low supply voltage (PS1).

Regarding claim 21, the "restore mechanism" is the multiplexor (208).

Regarding claim 22, the "state saving latch" is latch (24)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-6251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
05-22-03

TUAN T. LAM
PRIMARY EXAMINER